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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
| 09/742,171      | 12/19/2000  | Steven Teig          | SPLX.P0017          | 8567             |

23349 7590 08/27/2003

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| EXAMINER |
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THOMPSON, ANNETTE M

| ART UNIT | PAPER NUMBER |
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2825

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

AA

|                              |                               |                             |  |
|------------------------------|-------------------------------|-----------------------------|--|
| <b>Office Action Summary</b> | Application No.<br>09/742,171 | Applicant(s)<br>TEIG ET AL. |  |
|                              | Examiner<br>A. M. Thompson    | Art Unit<br>2825            |  |

-- **Th MAILING DATE of this communication appears on th cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 May 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 28-75 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 28-31, 34-36, 39-46, 49-51 and 54-57 is/are rejected.
- 7) ☒ Claim(s) 32, 33, 37, 38, 47, 48, 52, 53 and 58-75 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                          | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>10</u> . | 6) <input type="checkbox"/> Other:  |

### **DETAILED ACTION**

Applicant's Amendment and Response to Office Action has been reviewed and examined. The drawings and specification are amended. Claims 28, 29, 31, 43, 44, 58, 59, 67, and 68 are amended. Claims 28-75 are pending.

1. Applicant's Amendment is persuasive and obviates the objections and rejections of the prior office action. However, new grounds of rejections are herein introduced.

#### ***Claim Objections***

2. Claims 32, 47, 58, and 67 are objected to because of the following informalities: Pursuant to claims 32 and 47, "said slots" lacks antecedent basis. Pursuant to claim 58 and 67, these claims recite a method of pre-computing costs of placing circuit modules. However, the claims recite no limitation that appear related to the pre-computation of the costs of placing circuit modules. Claims dependent from objected to claims are likewise objected to. Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

4. A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Rejection of claims 28-31, 34-36, 39-46, 49-51 and 54-57**

5. Claims 28-31, 34-36, 39-46, 49-51 and 54-57 are rejected under 35 U.S.C. 102(e) as being anticipated by Rostoker et al. (Rostoker), U.S. Patent 5,822,214. Rostoker discloses cell architecture using hexagonal shaped cell and CAD methods relating to this type of architecture.

6. Pursuant to claim 28, Rostoker discloses a method of placing circuit modules in a region of an integrated circuit layout (col. 42, ll. 26-47 discloses floorplanning and placement) the method comprising partitioning the IC regions into several sub-regions, wherein a plurality of edges exist between said sub-regions, wherein a plurality of said edges are diagonal (col. 42, ll. 8-25 discloses partitioning; col. 41, ll. 55-65 discloses diagonal (or sixty degree edges); (see also col. 42, ll. 58-62); see also floorplanning and placement (col. 51, line 25 – col. 56, line 56);

selecting a net (col. 42, ll. 58-62);

identifying the set of sub-regions containing the circuit elements of the selected net;

identifying the edges, from the plurality of edges, intersected by at least one connection graph that represents a topology of one or more interconnect lines necessary for connecting the identified set of sub-regions, wherein at least one of the identified edges is diagonal (col.. 42, ll. 48-58; col. 56, line 56 to col. 59, line 63;

computing a placement cost by using the identified edges (col. 59, ll. 41-64).

7. Pursuant to claim 29, wherein a plurality of said edges are horizontal and a plurality are vertical (col. 41, ll. 58-64).

8. Pursuant to claim 30, wherein partitioning the IC region comprises using a set of partitioning lines to define sub-regions (col. 42, ll. 8-25).

9. Pursuant to claim 31, wherein the plurality of edges are defined based on a wiring model for the IC layout and on a partitioning structure defined by the partitioning lines (col. 58, line 36 to col. 59, line 65).

10. Pursuant to claim 34, further comprising changing the position of a circuit element of the selected net from one sub-region to another; identifying a new set of sub-regions that contain the elements of the selected net; identifying a new set of edges intersected by at least one new connection graph; computing a new placement cost by using the identified new set of edges (col. 60, line 11 to col. 61, line 36).

11. Pursuant to claim 35, further comprising for each particular net, identifying the set of sub-regions containing the circuit elements of the particular net; identifying a set of edges intersected by at least one connection graph that represents the topology of one or more interconnect lines (col. 59, ll. 5-63); computing a placement cost for the IC layout within said region based on the identified set of edges.

12. Pursuant to claim 36, further comprising changing the position of a particular circuit element from one sub-region to another; for each particular net that includes the element, identifying the sub-regions that contain the circuit elements of the particular net. . .computing a placement cost (col. 60, line 11 to col. 61, line 36).

13. Pursuant to claim 39 wherein identifying the edges comprises identifying the edges intersected by all optimal connection graphs for the selected net (col. 59, ll. 54-63).

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14. Pursuant to claim 40 wherein the connection graphs are determined to be optimal based on at least one particular selection criteria (col. 59, ll. 5-63).

15. Pursuant to claim 41, wherein the selection criterion is the length of the connection graph (col. 58, line 44 to col. 59, line 63).

16. Pursuant to claim 42, wherein another selection criterion for determining whether the connection graphs are optimal is the number of bends of the connection graphs (col. 57, line 7 to col. 59, line 21).

17. Pursuant to claims 43-46, 49-51, and 54-57, these claim incorporate similar limitations to claims 28-31, 34-36, and 39-42, already rejected supra, and therefore claims 43-46, 49-51, and 54-57 are likewise rejected based on the same reasoning.

#### ***Allowable Subject Matter***

18. Claims 32, 33, 37, 38, 47, 48, 52, 53 and 58-75 contain allowable subject matter.

19. The following is a statement of reasons for the indication of allowable subject matter: In a method of placing circuit modules involving diagonal edges and line paths, the prior art does not disclose an octagonal wiring model that has forty-two edges. Further, the prior art does not disclose storing a plurality of identified edges or line paths in a storage structure.

#### ***Conclusion***

20. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00

p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703) 306-3329.

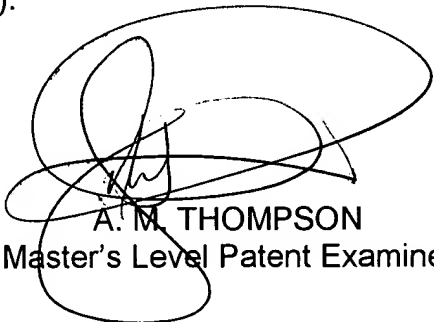
21. Responses to this action should be mailed to:

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).



A. M. THOMPSON  
Master's Level Patent Examiner